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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,291	12/19/2001	Thomas K. Johnston	SC11736TH	2738

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	4

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/025,291	JOHNSTON ET AL.
	Examiner	Art Unit
	John J Tabone, Jr.	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,12,16,19 and 23* is/are rejected.

7)☒ Claim(s) *4, 6-11, 13-15, 17, 18, 20-22, 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 12, 16, 19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peng (US-5524114).

Claims 1 and 16:

Peng substantially teaches the claimed voltage controlled oscillator clock 204 as part of an on chip phase-lock-loop driven by a system clock 220 (reference clock) and operating at a designated frequency (first frequency). Peng also teaches the frequency of the voltage controlled oscillator clock 204 is controlled by phase detector and reference multiplexer 206. During normal operation, the phase detector and reference multiplexer 206 locks the frequency of the voltage controlled oscillator clock 204 to either the system clock 220 frequency or some multiple thereof (second frequency higher than the first). (Col. 5, lines 41-54). Peng also discloses that the clock output 222 is connected to the input of clock and burst controller 208 (clock control circuitry). The burst controller 208 is utilized to gate off and control the number of clock pulses to the

combinational logic 212 during testing. (Col. 6, lines 10-12). Peng does not explicitly disclose a first and second storage devices for providing shift/capture and launch clocks, respectively. However, Peng does disclose the burst controller 208 (clock control circuitry) consists of logic that synchronously controls the number of pulses of controlled clock output 224. Peng suggests the launch and capture signals in that the burst controller 208 allows only two clock pulses from controlled clock output 224 to be applied to combinational logic 212: the first pulse clocks the scan-path test data into the combinational logic 212 (scan/capture), and the second pulse signals the end of the time in which combinational logic 212 may correctly operate on this test data (launch). (Col. 6, lines 52-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Peng's system such that the burst controller 208 (clock control circuitry) includes storage devices consisting of logic that synchronously controls the number of pulses of controlled clock output 224. The artisan would have been motivated to do so because this would enable the combinational logic 212 to be tested at a nominal operating speed with a low speed reference clock.

Claim 2:

Peng does not explicitly teach that the storage devices included in the burst controller 208 (clock control circuitry) (see claim 1 rejection) are circular shift registers, however, Peng does teach the burst controller 208 (clock control circuitry) consists of logic that synchronously controls the number of pulses of controlled clock output 224. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Peng's system such that the storage devices included in the burst

controller 208 (clock control circuitry) are circular shift registers because of the timing and the duration of the clock pulse it creates (See Fig. 3). The artisan would be motivated to do so because this would enable the combinational logic 212 to be tested at a nominal operating speed with a low speed reference clock.

Claim 3:

Peng teaches that during the test mode, the phase detector 206 uses the TCK 110 as the reference frequency and locks the frequency of the voltage controlled oscillator clock 204 thereto. The TCK 110 is normally at a lower frequency than the frequency of the voltage controlled oscillator clock 204. As an example, the voltage controlled oscillator clock 204 may operate at a frequency of 200 MHz and TCK 110 may operate at a frequency of 10 MHz. The frequency divider 210 (also part on the clock control circuit) will therefore divide by N, where N=200/10 or 20 (ratio of the high frequency clock divided by the reference clock). The purpose of the phase-lock-loop formed by the voltage controlled oscillator clock 204, frequency divider 210 and phase detector and reference multiplexer 206 is to synchronize the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110. The clock output 222 connects to the input of burst controller 208 (clock control circuitry). (Col. 6, lines 42-51).

Claim 5:

Peng teaches a modulo-N frequency divider 210 divides the clock output 222 frequency. Divided frequency output 218 is connected to the phase detector and reference multiplexer 206 (clock generator). The modulo-N frequency divider 210 may have a divide ratio N of any positive integer number, and may be programmed for

different values of N (integer divided version of high frequency clock). (Col. 5, lines, 49-60).

Claim 12:

Peng substantially teaches the claimed voltage controlled oscillator clock 204 as part of an on chip phase-lock-loop driven by a system clock 220 (reference clock) and operating at a designated frequency (first frequency). Peng also teaches the frequency of the voltage controlled oscillator clock 204 is controlled by phase detector and reference multiplexer 206. During normal operation, the phase detector and reference multiplexer 206 locks the frequency of the voltage controlled oscillator clock 204 to either the system clock 220 frequency or some multiple thereof (second frequency higher than the first). (Col. 5, lines 41-54). Also, it well known in the art that PLLs include a feedback connected from the output back to the input.

Claim 19:

Peng substantially teaches the claimed voltage controlled oscillator clock 204 as part of an on chip phase-lock-loop driven by a system clock 220 (reference clock) and operating at a designated frequency (first frequency). Peng also teaches the frequency of the voltage controlled oscillator clock 204 is controlled by phase detector and reference multiplexer 206. During normal operation, the phase detector and reference multiplexer 206 locks the frequency of the voltage controlled oscillator clock 204 to either the system clock 220 frequency or some multiple thereof (clock generator for generating a second frequency higher than the first). (Col. 5, lines 41-54). Peng also discloses that the clock output 222 is connected to the input of clock and burst controller

208 (global storage device). The burst controller 208 is utilized to gate off and control the number of clock pulses to the combinational logic 212 during testing. (Col. 6, lines 10-12). Peng does not explicitly disclose a global storage device for receiving the high frequency clock and a clock waveform generation circuit, however, Peng does disclose that the burst controller 208 (global storage device and clock waveform generation circuit) consists of logic that synchronously controls the number of pulses of controlled clock output 224 (sequence of state values). Peng also suggests the launch and capture signals in that the burst controller 208 allows only two clock pulses from controlled clock output 224 to be applied to combinational logic 212: the first pulse clocks the scan-path test data into the combinational logic 212 (scan/capture), and the second pulse signals the end of the time in which combinational logic 212 may correctly operate on this test data (launch). Peng further discloses the CTL 112 (test control signal) signal controls whether the logic circuit is in normal or test operation mode. (Col. 6, lines 31-41,52-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Peng's system such that the burst controller 208 (global storage device and clock waveform generation circuit) includes a storage device and a waveform generator consisting of logic that synchronously controls the number of pulses of controlled clock output 224. The artisan would have been motivated to do so because this would enable the combinational logic 212 to be tested at a nominal operating speed with a low speed reference clock.

The output logic circuitry for providing a divided version of the high frequency clock and a scan test clock is rejected per claim 5 above.

Claim 23:

This claim is rejected per claims 2 and 3 above.

Peng does not explicitly teach that the global storage device included in the burst controller 208 (global storage device) (see claim 19 rejection) is a circular shift register, however, Peng does teach the burst controller 208 (global storage device) consists of logic that synchronously controls the number of pulses of controlled clock output 224. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Peng's system such that the global storage device included in the burst controller 208 (global storage device) is a circular shift register because of the timing and the duration of the clock pulse it creates (See Fig. 3). The artisan would be motivated to do so because this would enable the combinational logic 212 to be tested at a nominal operating speed with a low speed reference clock. Peng teaches the ration of the high frequency clock and the reference clock in that during the test mode, the phase detector 206 uses the TCK 110 as the reference frequency and locks the frequency of the voltage controlled oscillator clock 204 thereto. The TCK 110 is normally at a lower frequency than the frequency of the voltage controlled oscillator clock 204. As an example, the voltage controlled oscillator clock 204 may operate at a frequency of 200 MHz and TCK 110 may operate at a frequency of 10 MHz. The frequency divider 210 (also part on the clock control circuit) will therefore divide by N, where N=200/10 or 20 (ratio of the high frequency clock divided by the reference clock). The purpose of the phase-lock-loop formed by the voltage controlled oscillator clock 204, frequency divider 210 and phase detector and reference multiplexer 206 is to synchronize the frequency

and phase of the internal clock output 222 to the frequency and phase of TCK 110. The clock output 222 connects to the input of burst controller 208 (global storage device). (Col. 6, lines 42-51).

Allowable Subject Matter

3. Claims 4, 6-11, 13-15, 17, 18, 20-22, 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's Statement of Reasons for Allowance:

The prior art of record teaches a clock generator that receives a reference clock from a low speed tests and generates a high frequency clock via voltage controlled oscillator, which is part of an on-chip phase-lock-loop (PLL) coupled to a phase detector for at-speed testing of a semiconductor circuit. The prior art of record also provides a clock control circuit via the burst controller 208, which generates the scan clock pulses. The high frequency clock is a ratio of the high frequency clock divided by the reference clock frequency. The prior art of record test for proper operation of the combinational logic 212 during a time period determined by the time between clock pulses 310a and 310b. Thus, the combinational logic 212 may be tested at its normal operating speed with a standard low speed logic tester 102. The prior art of record also adds that two or more clock pulses 310 may be utilized to test semiconductor devices at speed, and that the test cycles 304 and 306 may be combined, or additional test cycles added during testing of the combinational logic 212. Various high speed logic tests may be performed

on the combinational logic 212 by appropriately designed test scan-path logic 214 in combination with control, and phase locked test and system clock signals. The prior art of record quantitatively performs high speed tests on combinational logic 212 with a standard low speed logic tester 102 that includes testing of both the logic functions and the time in which these functions are performed; Peng (US-5524114) is one example of such prior arts. The prior arts of record, however, fail to teach, singly or in combination, varying the pulse-to-pulse delay between the launch and shift/capture clock while the frequency of the reference clock remains unchanged (claim 6); a third storage device for generating a second launch signal (claim 7); generating the high frequency operating clock in a divided and an inverse form during a non-test mode (claim 8); a feedback and delay circuit in the clock generator for providing the shift/capture clock as a feedback signal and phase matching (claim 9); the feedback signal is either an integer divided version of the high frequency operating clock during a normal mode of operation or as the output of the first storage device during a scan test mode of operation (claim 10); the shift/capture clock and the launch clock signals are delayed to maintain the same phase relationship with the feedback signal (claim 13).

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

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